CLAIMS

What is claimed is:

1. A method for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor, the method comprising:

executing an instruction within the processor;

receiving an interruption signal by the processor;

in response to receiving the interruption signal, determining whether a trap mode is to remain active during interruption processing;

in response to a determination that the trap mode is to be deactivated during interruption processing, deactivating the trap mode; and

invoking an interruption handler to perform interruption processing for the received interruption signal.

2. The method of claim 1 further comprising:

indicating whether the trap mode is active or inactive using a trap mode field within the processor.

3. The method of claim 2 wherein a first trap mode field indicates that a single-step trap mode is active.

4. The method of claim 2 wherein a second trap mode field indicates that a taken-branch trap mode is active.

5. The method of claim 1 further comprising:

indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor.

6. The method of claim 5 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

7. The method of claim 5 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

8. The method of claim 1 further comprising:

performing a trace operation prior to deactivating the trap mode.

9. The method of claim 1 further comprising:

reactivating the trap mode after interruption processing.

10. The method of claim 9 further comprising:

performing a trace operation after reactivating the trap mode.

11. A processor that performs operations specified by instructions fetched from a memory, the processor comprising:

means for maintaining a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are present within the processor;

means for fetching instructions from memory;

means for executing an instruction within the processor;

means for receiving a plurality of types of interruptions;

means for determining whether a trap mode is to remain active during interruption processing in response to receiving an interruption;

means for deactivating a trap mode in response to a determination that the trap mode is to be deactivated during interruption processing; and

means for invoking an interruption handler to perform interruption processing for a received interruption.

12. The processor of claim 11 further comprising:

means for maintaining a trap mode field within the processor to indicate whether the trap mode is active or inactive.

13. The processor of claim 12 wherein a first trap mode field indicates that a single-step trap mode is active.

14. The processor of claim 12 wherein a second trap mode field indicates that a taken-branch trap mode is active.

15. The processor of claim 11 further comprising:
means for maintaining a trap mode conditioning field within the processor to indicate whether a trap mode is to remain active during interruption processing.

16. The processor of claim 15 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

17. The processor of claim 15 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

18. The processor of claim 11 further comprising:
means for performing a trace operation prior to deactivating the trap mode.

19. The processor of claim 11 further comprising:
means for reactivating the trap mode after interruption processing.

20. The processor of claim 19 further comprising:
means for performing a trace operation after reactivating the trap mode.

21. A computer program product in a computer-readable medium for use in a data processing system for processing an instruction within a processor, wherein the processor processes a plurality of types of interruptions, and wherein the processor comprises a plurality of register fields for indicating one or more conditions, statuses, and/or modes that are active within the processor, the computer program product comprising:

means for executing an instruction within the processor;

means for receiving an interruption signal by the processor;

means for determining whether a trap mode is to remain active during interruption processing in response to receiving the interruption signal;

means for deactivating the trap mode in response to a determination that the trap mode is to be deactivated during interruption processing; and

means for invoking an interruption handler to perform interruption processing for the received interruption signal.

22. The computer program product of claim 21 further comprising:

means for indicating whether the trap mode is active or inactive using a trap mode field within the processor.

23. The computer program product of claim 22 wherein a first trap mode field indicates that a single-step trap mode is active.

24. The computer program product of claim 22 wherein a second trap mode field indicates that a taken-branch trap mode is active.

25. The computer program product of claim 21 further comprising:

means for indicating whether a trap mode is to remain active during interruption processing using a trap mode conditioning field within the processor.

26. The computer program product of claim 25 wherein a first trap mode conditioning field conditions activity of a single-step trap mode.

27. The computer program product of claim 25 wherein a second trap mode conditioning field conditions activity of a taken-branch trap mode.

28. The computer program product of claim 21 further comprising:

means for performing a trace operation prior to deactivating the trap mode.

29. The computer program product of claim 21 further comprising:

means for reactivating the trap mode after interruption processing.

30. The computer program product of claim 29 further comprising:

means for performing a trace operation after reactivating the trap mode.